Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **N. EA**
2. **A0A**
3. **A1A**
4. **N. O0A**
5. **N. O1A**
6. **N. O2A**
7. **N. O3A**
8. **GND**
9. **N. O3B**
10. **N. O2B**
11. **N. O1B**
12. **N. O0B**
13. **A1B**
14. **A0B**
15. **N. EB**
16. **VCC**

**.049”**

**3**

**N/A**

**4**

**5**

**6**

**7**

**2 1 16 15**

**14**

**13**

**12**

**11**

**10**

**N/A 8 9**

**F139**

**MASK**

**REF**

**.051”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: F139**

**APPROVED BY: DK DIE SIZE .049” X .051” DATE: 8/18/21**

**MFG: MOTOROLA THICKNESS .013” P/N: 54F139**

**DG 10.1.2**

#### Rev B, 7/1